DS-02-020

January 13, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

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Subject: Serial No. 10/614,663 07/07/03

Rainer Krenzke et al.

COMPARATOR WITH HIGH-VOLTAGE INPUTS IN AN EXTENDED CMOS PROCESS FOR HIGHER VOLTAGE LEVELS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

U.S. Patent 6,037,890 to Glass et al., "Ultra High Speed, Low Power, Flash A/D Converter Utilizing a Current Mode Regenerative Comparator," discloses a method and apparatus for performing analog to digital conversion.

U.S. Patent 4,114,149 to Kendall, "Current Comparator for an Improved Analog-to-Digital Converter Method and Apparatus," discusses a circuit for sensing the polarity of a net input current at a current summing node.

U.S. Patent 5,089,871 to Fujihara, "Increased Voltage MOS Semiconductor Device," discloses an increased operating voltage MOS semiconductor device.

U.S. Patent 6,232,801 to Khoury et al., "Comparators and Comparison Methods," discusses comparators, memory devices, comparison methods and memory reading methods.

U.S. Patent 6,208,174 to Hopkins, "High-speed Comparator Systems and Methods with Enhanced Noise Rejection," discusses comparator systems and methods that isolate their input and output processes from each other.

U.S. Patent 5,600,269 to Song et al., "Low Power Consumption Comparator Circuit," discloses a low power-consumption type comparator circuit.

U.S. Patent Application Publication US 2001/0007443 A1, to Ono, "Differential Amplifier, Comparator, and A/D Converter," discusses an OTA circuit disposed between a differential pair composed of NMOS transistors and an NMOS follower transistor that composes a output buffer circuit.

U.S. Patent 5,589,785 to Garavan, "Low-Voltage CMOS Comparator," discloses a MOS comparator which includes a capacitor connected in an electrical path between two amplification stages.

U.S. Patent 6,157,220 to Broekaert, "High-Speed Differential Comparator," discloses a high-speed differential comparator.

U.S. Patent 4,199,733 to Schade, Jr., "Extended-drain MOS Mirrors," discusses an improved current amplifier, of the type having input, output and common terminals.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
DS-02-020	10/614,663
Applicant: Rainer Kronzke et al.	
Filing Date: 07/07/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6037890	3/14/00	Glass et al.	341	159	9/30/97
	4114149	9/12/78	Kendall	340	347	7/19/76
	5089871	2/18/92	Fujihara	357	23.8	7/3/90
	6232801	5/15/01	Khoury et al.	327	57	8/4/99
	6208174	3/27/01	Hopkins	327	65	12/14/99
	5600269	2/4/97	Song et al.	327	52	12/2/94
	5589785	12/31/96	Garavan	327	63	6/7/95
	6157220	12/5/00	Broekaert	327	65	1/6/99
	4199733	4/22/80	Schade, Jr.	330	277	9/25/78

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

-	U.S. Patent App. Pub. US2001/0007443 A1 to Ono, "Differential Amplifier, Comparator, and A/D Converter", Pub. Date 7/12/01, U.S. Class 341/159, Filed 12/21/00.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.